CUSTOMER NOTIFICATION

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CP(K), O

QB-MINI2

使用前需知

使用 QB-MINI2 需知

本文件描述下述事项。使用MINICUBE2时的注意事项,请参阅QB-MINI2(下文称MINICUBE2)

- 关于目标板不限制,但MINI2限制
- 目标板和MINICUBE2同时限制,但计划更正MINICUBE2方面
- MINICUBE2支持的器件

关于目标器件所受的限制,参阅下述文件.

- 目标器件的用户手册
- 目标器件限制通知文件

1. 产品版本

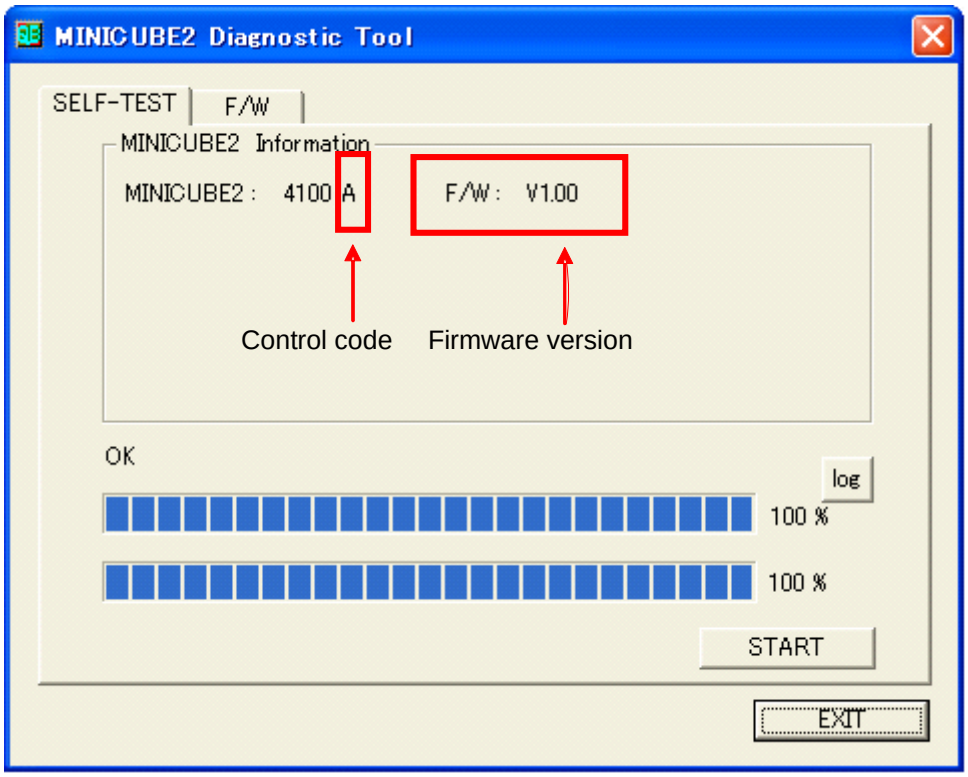
控制码[注1]	固件[注2]	备注
A	V1.00	新公布
	V2.00	支持 V850 微处理器
	V3.00	支持 78K0S 微处理器
	V4.00	支持 78K0R 微处理器
	V4.01	
	V4.03	

注 1. 本"控制码"是英文字母编码，用来确认MINICUBE2的硬件。 标签贴在MINI2的底部，它是10位序列号由左算来的第2位。

如果产品被更新MINIUBE2的自检工具可以检测此控制码

2. 固化件（F/W）的版本是嵌入MINICUBE2内的一个控制程序,F/W版本显示为VX,XX(X表示任何数目).版本可用MINICUBE2的自检工具检查(参阅下图1-1)

图 1-1. 检查控制码和固化版本



2. 产品历史

表 2-1是关于 MINICUBE2 限制和更改/新增规格表

Table 2-1. 限制和更改/新增规格表

No.	目的器件	Note D/P	更改/新增规格和限制	控制码 A F/W 版本 V1.00	V2.00	V3.00	V4.00	V4.01	
1	78K0	D	内部高速RAM值在重置后无效	×	×	×	×	×	×
2	V850	D	关于看门狗时钟限制	–	×	×	×	×	×
3	V850	D	子时钟操作时的中断限制	–	×	×	×	×	×
4	V850	D	在内存服务时的中断限制	–	×	×	×	×	×
5	V850	D	限制重置向量处理功能的限制	–	×	×	×	×	×
6	V850	D	限制需要一定步骤,重写暂存器的限制	–	×	×	×	×	×
7	V850	D	限制当一个重置产生	–	×	×	×	×	×
8	78K0S	D	限制时钟在6MHZ或更低操作时的限制	–	–	×	֍	֍	֍
9	78K0S	D	限制当时钟在10M操作时的下载限制	–	–	×	×	֍	֍
10	78K0S	D	限制暂存器值的显示	–	–	×	֍	֍	֍
11	78K0R	D	限制中断夹在CPU时针低于2MHZ的限制	–	–	–	×	×	
12	78K0R	D	限制在1-WIRE模式时,调试时钟功能的限制	–	–	–	×	×	֍
13	78K0R	D	限制在程序下载时的无效操作	–	–	–	×	×	֍
14	78K0R	D	QB-MINI2在使用USB1.1	–	–	–	×	×	֍
15	78K0	D	操作在20MHZ或更高	×	×	×	×	×	֍
16	78K0R	D	限制通用暂存器在重置后的限制	–	–	–	×	×	×
17	78K0R	D	规格更改/新加来符合固化件优化	–	–	–	×	×	֍
18	78K0R	D	硬件中断	–	–	–	×	×	×

֍: 限制无效或已修正。适用于已更改或新增规格。

△: 限制被部分校正。

×: 限制生效,目标器件不支持.

–: 不相关或目标器件不支持

注 D:适用于调试时, P: 适用于编程时.

备注：永久限制表示不计划更正的限制.

3. 限制和更改规格的细节

第一 内部高速RAM值在重置后变成无效

[目标器件] 78K0

[Description]

当程序正在执行时,重置脚位输入的重置执行,内部高速RAM区显示如下.

- 5 字节 由 FECBh到FECFh

(目标断电时选择允许，在配置对话框中)

- 10 字节由FEC9h到 FECFh 和 FEDDh 到FEDFh

(不允许目标断电,在配置对话框中)

[工作]

无工作区.

第二 关于看门狗时钟的限制r

[目标时钟] V850

[叙述]

看门狗是强制中断.由调试监控程序,因此不要让已不选字节的设置.无法停止看门狗时钟,可选字节的设置,参阅用户手册上面目标器件

[工作区]

无工作区.

第三 子时钟操作时的中断限制

[目标器件] V850

[叙述]

通讯模式.MINICUBE2和目标器件是UART时,主时钟停止.监控控制程序.手动把时钟改为主时钟.器件继续用主时钟运作.即便再恢复执行.中断时时钟运作是否由子时钟改为主时钟,祝主时钟在调试器配置对话框内的设定范围.

[工作区]

无工作区.

第四 Restriction 关于中断.在闪存群集服务时

[目标器件] V850

[叙述]

当中断发生,在闪存群集服务时, 地址是不可预计的.这在调试时中断也适用.例如:用在假RRM功能

[工作区]

重置目标器件并再执行程序.

第五 重置向量处理功能

[目标器件] V850

[叙述]

不支持此重置向的处理功能.

[工作区]

无工作区.

第六 需要一定步骤重写需存器

[目标器件] V850

[叙述]

外围I/O寄存器(PCC和CKC除外)无法在调试的I/O寄存器窗口或数似,再重写入.需要一定步骤才能再写入的

[工作区]

无工作区.

第七 中断产生时

[目标器件] V850

[叙述]

当外部光重置不被罩遮或内部中断产生时

[工作区]

无工作区.

第八 调试在时钟运行在6MHZ更低时

[目标器件] 78K0S

[描述]

本调试器不启动,当目标器件运行在6MHZ或更低时

[工作区]

无工作区. 此项在固化体V4.00时已被更正.

第九 在运作时钟为10MHZ时的下载限制

[目标器件] 78K0S

[叙述]

在运作时钟为10MHZ时的下载限制,将产生错误,在程序下载而且下载无法完成

[工作区]

无工作区，此项已在固化件V4.01更正.如果你正在NEC电子调试ID78K0S-QB，请改为V2.90或者更新版.

第十 寄存器限制

[目标器件] 78K0S

[叙述]

寄存器值可能显示不正常，当调试器中断发生时。

[工作区]

无工作区，此项已在固化件V4.00被更改。

第十一 CPU时钟低过2 MHz时断点限制

[目标器件] 78K0R

[叙述]

中断产生.在 CPU时钟(fclk)运行.低过2MHz在PER0和PER1寄存器值被认为0的,内部闪存不能再被写入。导致下述操作不能执行

<1> 写入内部闪存

<2> 放置或取消软件断点

<3> 由软件设置位置开始执行

<4> 由软件断点设置位置单步运行,

<5> 执行单步后回返,执行

<6> 执行到此

<7> 如在闪存区段的对话框允许设置.下述操作无法进行

(a) 设置改变或取消硬件断点

(b) 遮断或允许内部重置

(c) 外围中断的开或关

[工作区]

无工作区。在CPU时钟低于 2 MHz运行时的断点设置，使用硬件中断而非软件中断。

在固化件为 V4.03时，此限制有部分被更正。使用此更正时，请使用NEC电子调试器D78K0R-QB V3.30或更新版，规格将被改正。

使得在闪存可被读写的频率运作时可以启动频率.

[改正]

当在闪存无法被写的时钟频率时,寄存器设置在闪存可被再写入时自动回复,为闭免频率被自动开或关,选择用户,在监控器的时钟和不允许在闪存编程区,在ID78K0R-QB的配置对话框,然而 <1>～ <7>不再被执行.

第十二 单线模式下调试器的时间测量功能

[目标器件] 78K0R

[叙述]

当用单线模式来调试时(在目标器件连接这块配置对话框选择TOOLO) ，执行中断，执行时间。测量的准确度是以粗略的10毫秒为单位。规定的精度是100微秒。

[工作区]

用双线模式来执行调试时 (TOOL0 + TOOL1).

此项在版本 V4.03已改正。如果你使用的是NEC电子调试器 ID78K0R-QB,请转到ID78K0R-QB V3.30 或更新版本。

第十三 关于程序下载的无效选择限制

[目标器件] 78K0R

[叙述]

当变量向量(addresses 0 和 1) 被指定到0x0100更低的地址，调试器程序被下载后无法再正常运作.. 更具体的说是:运行时非法中断立即出现，源文件窗口无法打开等.

[工作区]

用户程序地址的重置向量,请指定在高速f 0x0100 .

此项在固化体V4.03中改正.如果你是使用NEC电子调试器ID78K0R-QB请转换到ID78K0R-QB V3.30或更新.

第十四 QB-MINI2使用USB 1.1的限制

[目标器件] 78K0R

[叙述]

如果是使用USB 1.1时调试器运作可能不正常。

[工作区]

无工作区。此项在固化件V4.03中已被更改。

第十五 在20HZ时或更高频率操作时的限制

[目标器件] 78K0R

[叙述]

当 QB-MINI2在20HZ时或更高频率操作时， 下载或处理改变内存容量可能失败。

[工作区]

低于20HZ时操作， 执行下载或处理改变内存容量。此项在固化件V4.03中已被更改。

No. 16 Restriction on general-purpose registers after reset

[Target device] 78K0R

[Description]

After reset in standby mode, the general register contents are not retained.

[Workaround]

There is no workaround.

No. 17 Specifications changed/added in conjunction with firmware optimization

[Target device] 78K0R

[Description]

The specifications shown below have been changed or added in conjunction with firmware optimization. See **5. Changes to User's Manual** for information on changes in the MINICUBE2 user's manual in conjunction with this modification.

This item has been implemented in firmware V4.03. To apply this correction, use the NEC Electronics debugger ID78K0R-QB V3.30 or later.

<1> The debugger operation speed has been improved by improving the MINICUBE2 firmware processing.

<2> The operation speed in 1-wire mode has been improved to be equalized with that in 2-wire mode. See **5.1** for information on changes in the MINICUBE2 user's manual.

<3> For a case when the pseudo real-time monitor function (RRM function) is not used during debugging in 2-wire mode, the occupied size of the debug monitor program allocated to the last block in the internal ROM has been reduced from 1 KB to 88 bytes.

<4> See **5.2** for details and information on changes in the MINICUBE2 user's manual.

<5> Instructions that perform two instructions during step-wise execution have been modified so as to perform only one instruction.
See **5.3** for details and information on changes in the MINICUBE2 user's manual.

<6> The option byte setting (C1H) for the LVI default start function is now the same regardless of whether MINICUBE2 is connected.
See **5.4** for details and information on changes in the MINICUBE2 user's manual.

<7> Debugger operations for rewriting the flash memory (download, software break setting, etc.), which were not possible while the target microcontroller cannot rewrite the flash memory, are now available by changing the specification so that the debugger automatically enables rewriting of the flash memory to enable such operations. (Correction of restriction No. 11 is also reflected to this change). In addition, the debugger now outputs an error when the voltage is too low and when flash memory rewriting is prohibited.
See **5.5** for details and information on changes in the MINICUBE2 user's manual.

<8> A break, which was generated if STOP mode is entered when the pseudo RRM function is used, is now prevented by releasing the STOP mode.
See **5.6** for details and information on changes in the MINICUBE2 user's manual.

No. 18 Restriction on hardware breaks

[Target device] 78K0R

[Description]

A hardware break occurs at an address several instructions after the specified point. This applies to both instruction fetch and data access. If any of the following debugger operations <1> to <3> is performed while the flash memory cannot be rewritten, a hardware break occurs at an address several instructions after the specified point.

<1> Step-wise execution

<2> Return Out execution

<3> Come Here

[Workaround]

There is no workaround.

4. Supported Devices

The devices that are supported by MINICUBE2, as of the issue date of this document, are described in the following. The changes in this edition are indicated by bold face print.

Information on the supported devices is also available on the following MINICUBE2 website.

URL http://www.necel.com/micro/english/product/sc/allflash/minicube2.html

4.1 78K0 microcontrollers

The following table lists the support status for 78K0 microcontrollers. Support for the target device also differs depending on the version of the development tools.

Supported Device	On-Chip Debugging				Flash Memory Programming			
	Firmware Version	ID78K0-QB Version	Device File Package	Version	Firmware Version	QBP Version	Parameter File Package	Version
78K0/LE2 78K0/LF2 78K0/LG2	V1.00	V2.93	DF780397	V1.01	V1.00	V1.00	PRM78F0397	V1.02
78K0/KB2 78K0/KC2 78K0/KD2 78K0/KE2 78K0/KF2	V1.00	V2.93	DF780547	V2.10	V1.00	V1.00	PRM78F0547	V1.05
78K0/KB1+ 78K0/KC1+ 78K0/KD1+ 78K0/KE1+ 78K0/KF1+	**V4.01**	**V2.94**	**DF780148H**	**V3.00**	V1.00	V1.00	PRM78F0148H	V1.12
μPD78F0731	**V4.01**	**V2.94**	**DF780731**	**V1.00**	V1.00	V1.00	PRM78F0731	V1.01
78K0/FC2 78K0/FE2 78K0/FF2	**V4.01**	**V2.94**	**DF780893**	**V1.00**	V1.00	V1.00	PRM78F0893	V1.03
78K0/FC1+ 78K0/FE1+ 78K0/FF1+	**V4.01**	**V2.94**	**DF780876**	**V1.10**	V1.00	V1.00	PRM78F0876	V1.11
μPD78F800xH	Not supported				V1.00	V1.00	PRM78F8006H	V1.00
μPD78F801x	Not supported				V1.00	V1.00	PRM78F8016	V1.01
μPD78F802x	Not supported				V1.00	V1.00	PRM78F8020	V1.01
μPD78F0712 μPD78F0714	**V4.01**	**V2.94**	**DF780714**	**V1.10**	V1.00	V1.00	PRM78F0714	V1.11
μPD78F0862 μPD78F0862A	Not supported				V1.00	V1.00	PRM78F0862	V1.11

4.2 V850 microcontrollers

The following table lists the support status for V850 microcontrollers. Support for the target device also differs depending on the version of the development tools. Check the serial interface that can be used as a communication interface between MINICUBE2 and the target device.

(1/2)

Supported Device	On-Chip Debugging					Flash Memory Programming			
	Supported Serial Interface	Firmware Version	ID850QB Version	Device File Package	Version	Firmware Version	QBP Version	Parameter File Package	Version
V850ES/HE2	UARTA0 CSIB0	V2.00	V3.20	DF703712	V1.10	V2.00	V1.00	PRM70F3712	V1.00
V850ES/HF2									
V850ES/HG2									
V850ES/HJ2									
V850ES/IE2	UARTA0 CSIB0	V2.00	V3.20	DF703714	V1.00	V2.00	V1.00	PRM70F3714	V1.00
V850ES/JG2	UARTA0 CSIB0/CSIB3	V2.00	V3.20	DF703724	V1.00	V2.00	V1.00	PRM70F3724	V1.00
V850ES/JJ2									
V850ES/KE2	UART0 CSI0	V2.00	V3.20	DF703734	V1.00	V2.00	V1.00	PRM70F3734	V1.01
V850ES/KF2									
V850ES/KG2									
V850ES/KJ2									
V850ES/KE1	Not supported					V2.00	V1.00	PRM70F3218H[Note]	V1.11
V850ES/KF1									
V850ES/KG1									
V850ES/KJ1									
V850ES/KE1+	Not supported					V2.00	V1.00	PRM70F3318H	V1.11
V850ES/KF1+									
V850ES/KG1+									
V850ES/KJ1+									
V850ES/FE2	Not supported					V2.00	V1.00	PRM70F3239	V1.12
V850ES/FF2									
V850ES/FG2									
V850ES/FJ2									
V850ES/FE3	**Not supported**					**V4.00**	**V2.00**	**PRM70F3385**	**V1.00**
V850ES/FF3									
V850ES/FG3									
V850ES/FJ3									
V850ES/FK3									
V850E/IA3	Not supported					V2.00	V1.00	PRM70F3184	V2.10
V850E/IA4	Not supported					V2.00	V1.00	PRM70F3186	V2.10
V850ES/IK1	Not supported					V2.00	V1.00	PRM70F3329	V1.20

Note Supported only in single-power-supply products (product name suffixed by H)

(2/2)

Supported Device	On-Chip Debugging					Flash Memory Programming			
	Supported Serial Interface	Firmware Version	ID850QB Version	Device File Package	Version	Firmware Version	QBP Version	Parameter File Package	Version
V850ES/SG2 V850ES/SJ2	Not supported					V2.00	V1.00	PRM70F3288	V1.11
V850ES/SG3 V850ES/SJ3	Not supported					V2.00	V1.00	PRM70F3368	**V1.01**
V850ES/DG2 V850ES/DJ2	Not supported					V2.00	V1.00	PRM70F3325	V1.10
V850ES/MA3	Not supported					V2.00	V1.00	PRM70F3134A	**V1.20**
V850ES/SV2	Not supported					V2.00	V1.00	PRM70F3166	V1.10
V850ES/RS1	Not supported					V2.00	V1.00	PRM70F3403	V1.10
V850ES/RS2	Not supported					V2.00	V1.00	PRM70F3746	V1.10

4.3 78K0S microcontrollers

The following table lists the support status for 78K0S microcontrollers. Support for the target device also differs depending on the version of the development tools. Check the external interrupt pins that can be used as a communication interface between MINICUBE2 and the target device.

Supported Device	On-Chip Debugging					Flash Memory Programming			
	Supported Serial Interface	Firmware Version	ID78K0S-QB Version	Device File Package	Version	Firmware Version	QBP Version	Parameter File Package	Version
78K0S/KU1+	INTP1	V4.01	V2.90	DF789234	V2.11	V3.00	V1.00	PRM78F9234	**V1.06**
78K0S/KY1+									
78K0S/KA1+	INTP3								
78K0S/KB1+									
μPD78F9334	Not supported					V3.00	V1.00	PRM78F9334	V1.00

4.4 78K0R microcontrollers

The following table lists the support status for 78K0R microcontrollers. Support for the target device also differs depending on the version of the development tools.

Supported Device	On-Chip Debugging				Flash Memory Programming			
	Firmware Version	ID78K0R-QB Version	Device File Package	Version	Firmware Version	QBP Version	Parameter File Package	Version
78K0R/KE3	**V4.03**	**V3.30**	**DF781188**	**V3.00**	V4.00	V2.00	**PRM78F1188**	**V1.00**
78K0R/KF3								
78K0R/KG3								
78K0R/KH3								
78K0R/KJ3								

5. Changes to User's Manual

This section describes the differences in the MINICUBE2 user's manual (document number: U18371EJ1), which are caused in conjunction with specification changes and additions. Correction of erroneous descriptions is also described.

5.1 Improvement of operation speed in 1-wire mode (78K0R)

- Location 1

  Figure 6-1 in **6.1 Target System Design** (p. 134)

- Before change

Communication Mode	Flash Programming Function	Debugging Function
1-wire mode	Available	Pseudo real-time RAM monitor (RRM) function: Unavailable DMM function (writing to memory during RUN): Unavailable
2-wire mode	Available	Pseudo real-time RAM monitor (RRM) function: Available DMM function (writing to memory during RUN): Available

- After change

Communication Mode	Flash Programming Function	Debugging Function
1-wire mode	Available	Pseudo real-time RAM monitor (RRM) function: Unavailable
2-wire mode	Available	Pseudo real-time RAM monitor (RRM) function: Available

- Location 2

  (12) in **6.2.6 Cautions on debugging** (p. 154)

- Before change

Note the following points when debugging is performed in 1-wire mode (selected by choosing TOOL0 in the Target Device Connection area in the Configuration dialog box of the debugger).

<1> The debugger operation speed is two to four times slower than that in 2-wire mode.

<2> When the internal high-speed oscillator is used for the CPU operating clock, breaks may not occur normally if the frequency variation between debugger startup and break occurrence (except for when changing the CKC register) is too large. This situation may occur when the variation of operating voltage or temperature is too large.

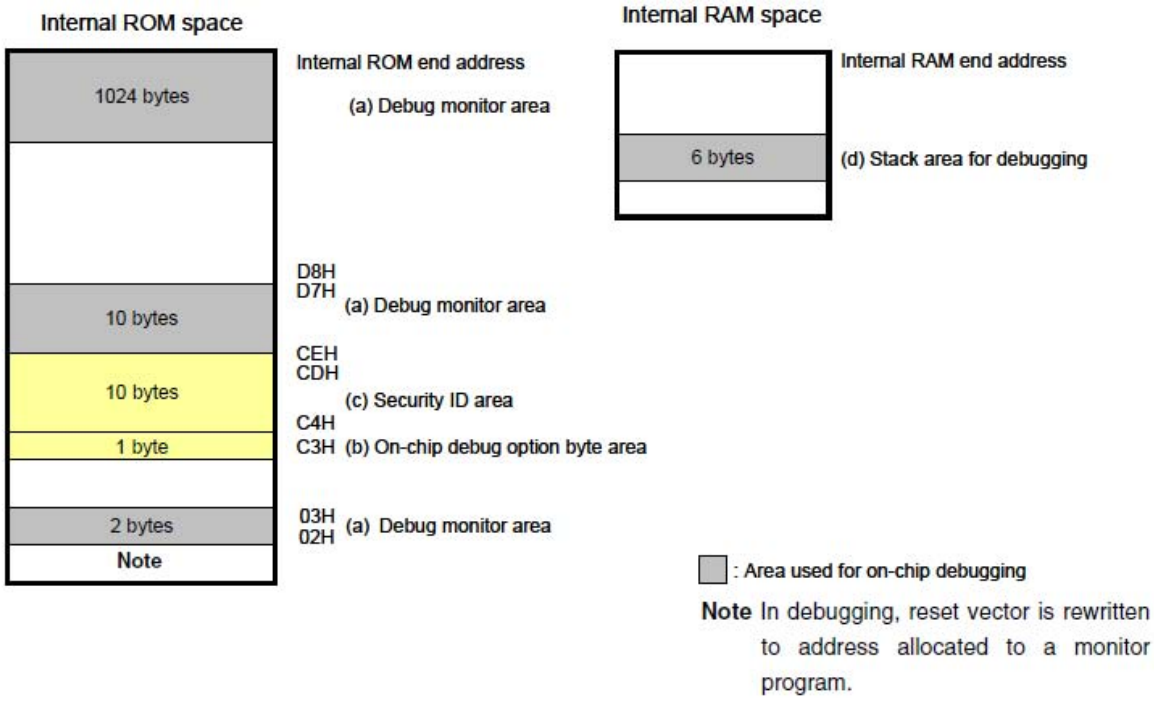
- After change

In the condition that debugging is performed in 1-wire mode (selected by choosing TOOL0 in the Target Device Connection area in the Configuration dialog box of the debugger), when the internal high-speed oscillator is used for the CPU operating clock, breaks may not occur normally if the frequency variation between debugger startup and break occurrence (except for when changing the register) is too large. This situation may occur when the variation of operating voltage or temperature is too large.

5.2 Reduction of monitor program occupation size in 2-wire mode (78K0R)

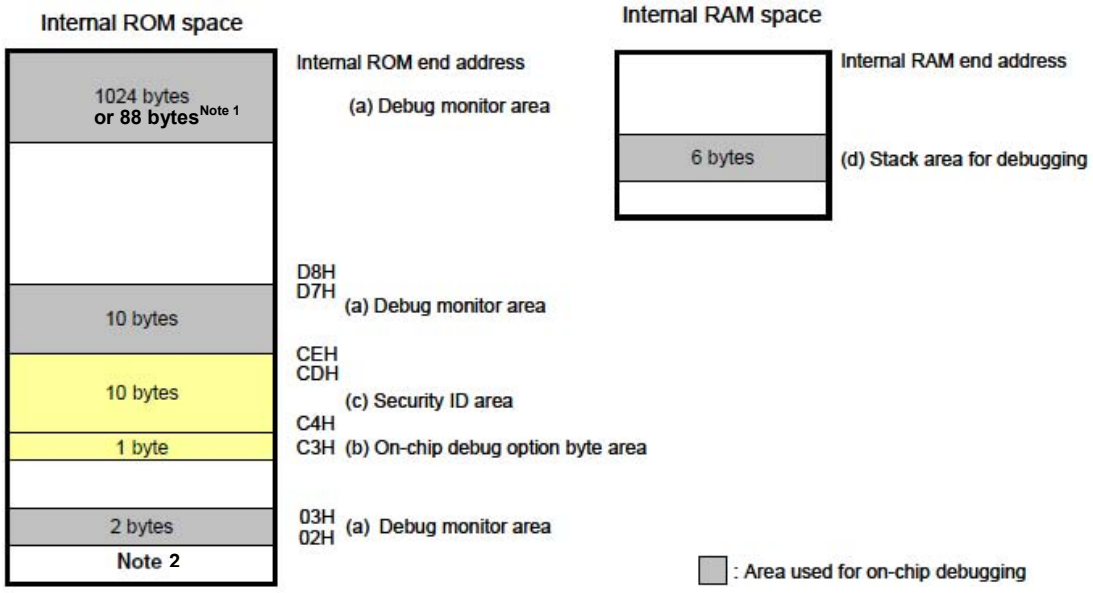
- Location 1

Figure 6-11 in **6.2.5 Securing of user resources and setting of security ID** … (p. 146)



Note In debugging, reset vector is rewritten to address allocated to a monitor program.

- After change (addition of **Note 1**)



Notes 1. When the pseudo RRM function is not used during 2-wire mode, it will be 88 bytes.

2. During debugging, a reset vector is overwritten by the address where the monitor program is allocated.

➢ Location 2

(a) in **6.2.5 Securing of user resources and setting of security ID,** … (p. 147)

➢ Before change

This user programs or data must not be placed in an area of 22 bytes near the on-chip debug option byte, and an area of 1,024 bytes before the internal ROM end address. In addition, reset vector is rewritten to address allocated to a monitor program.

➢ After change

This user programs or data must not be placed in an area of 22 bytes near the on-chip debug option byte, and an area of 1,024 bytes[Note] before the internal ROM end address. In addition, reset vector is rewritten to address allocated to a monitor program.

Note It is an area of 88 bytes when the pseudo RRM function is not used during debugging in 2-wire mode. If the internal ROM end address is 0x3FFFF, a monitor program of 88 bytes is allocated to the area from 0x3FFA8 to 0x3FFFF.

5.3 Improvement on Step execution (78K0R)

➢ Location

(5) in **6.2.6 Cautions on debugging** (p. 152)

➢ Deleted description

(5) Step execution

If step execution is performed for the following instructions, an extra instruction is executed.

a. RETI/RETB instruction

Immediately after returning from the interrupt servicing, an instruction is executed and then the execution breaks.

b. Conditional skip instruction (condition is not satisfied)

The instruction following the conditional skip instruction is executed and then the execution breaks.

5.4 Changes on operation specification of LVI default start function (78K0R)

➢ Location

(8) LVI default start function setting in **6.2.6 Cautions on debugging** (p. 152)

➢ Before change

(8) LVI default start function setting (address C1H)

The LVI setting at address C1H in the internal flash memory during debugging is set as follows.

- When MINICUBE2 is connected: The LVI default start function is available.
- When MINICUBE2 is not connected: The LVI default start function is unavailable.

➢ After change

(8) LVI default start function setting (address C1H)

During debugging, the debug monitor program stops the LVI default start function at address C1H. Consequently, the LVI default start function is kept stopped even after debugging is completed, unless the setting to address C1H is changed through flash programming.

5.5 Changes to debugger operation while flash memory cannot be rewritten (78K0R)

➢ Location

(11) in **6.2.6 Cautions on debugging** (p. 153)

➢ Before change

(11) Operation at voltage with which flash memory cannot be written

Do not perform the following operations at a voltage with which flash memory cannot be written. Otherwise, the subsequent operation may be unstable.

<1> Writing to internal flash memory

:

<7> If Permit is selected in the Flash Programming area in the Configuration dialog box, the following operations cannot be performed.

a) Setting, changing, or canceling of hardware breaks

b) Masking/unmasking of internal reset

c) Switching of peripheral breaks

➢ After change

(11) Operation while flash memory cannot be written

If any of the following debugger operations <1> to <7>, which involve flash memory rewriting, is performed while flash memory cannot be rewritten, the debugger automatically changes the register setting so as to enable flash memory rewriting, and restores the register setting after the operation is completed. If any of the following operations <1> to <7> is performed while flash memory rewriting has been disabled or operation is performed at a voltage with which flash memory cannot be rewritten, however, the debugger outputs an error and the operation is ignored.

To prevent the flash memory from being rewritten, select “Not Permit” in the Flash Programming area in the ID78K0R-QB Configuration dialog box. To prevent the frequency from being switched automatically, select “User” in the Monitor Clock area in the Flash Programming area in the ID78K0R-QB Configuration dialog box.

<1> Writing to internal flash memory

<2> Setting or canceling of software breakpoint

<3> Starting execution at the set software breakpoint position

<4> Step-wise execution at the set software breakpoint position

<5> Step-wise execution, Return Out execution

<6> Come Here

<7> If Permit is selected in the Flash Programming area in the Configuration dialog box, the following operations cannot be performed.

a) Setting, changing, or canceling of hardware breaks

b) Masking/unmasking of internal reset

c) Switching of peripheral breaks

5.6 Changes in specifications for using pseudo RRM function (78K0R)

➢ Location

(13) Pseudo real-time monitor function in **6.2.6 Cautions on debugging** (p. 154)

➢ Before change

(13) Pseudo real-time monitor function

Note the following points when using the pseudo real-time monitor function.

<1> The HALT mode is released during monitoring.

<2> The pseudo real-time monitor function does not operate while the CPU operating clock is stopped.

<3> A break may occur if the STOP mode is entered while the pseudo real-time monitor function being used.

➢ After change

(13) Pseudo real-time monitor function

Note the following points when using the pseudo real-time monitor function.

<1> Standby mode (HALT or STOP) may be cancelled during monitoring.

<2> The pseudo real-time monitor function does not operate while the CPU operating clock is stopped.

5.7 Cautions on flash programming interface (78K0)

➢ Location

Table 4-5 in **4.1.2 Circuit connection examples** (p. 54)

➢ Before change

Usage	Connector Used	Programming Interface	Debug Interface	Operating Clock Source Used by Target Device	FLMD1 pin[Note 1]	Refer to:
(1)	16-pin connector	UART	X1, X2	Internal high-speed oscillator (X1 oscillator not used)	Not provided	Figure 4-3
:						
(3)	16-pin connector	UART	-	-	-	Figure 4-11

Notes 1. Refer to the target device's user's manual to confirm whether an FLMD1 pin is provided.

2. The debug interface pin name varies depending on the target device. For details, confirm the target device's user's manual.

➢ After change (addition of **Note 3**)

Usage	Connector Used	Programming Interface	Debug Interface	Operating Clock Source Used by Target Device	FLMD1 pin[Note 1]	Refer to:
(1)	16-pin connector	UART[Note 3]	X1, X2	Internal high-speed oscillator (X1 oscillator not used)	Not provided	Figure 4-3
:						
(3)	16-pin connector	UART[Note 3]	-	-	-	Figure 4-11

Notes 1. Refer to the target device's user's manual to confirm whether an FLMD1 pin is provided.

2. The debug interface pin name varies depending on the target device. For details, confirm the target device's user's manual.

3. For the usable channels (such as CART0 and UART6), see the target device's user's manual (flash memory chapter).

5.8 POC functions (78K0)

➢ Location 1

(4) in **4.1.3 Reset pin** (p. 68)

➢ Before change

(4) Resetting the target device by power-on clear (POC) only

Figure 4-18 illustrates the circuit connection for the case where the target device is only reset via POC without using the reset pin. RESET_OUT is valid only when the debugger is running or during flash programming.

The operation is not guaranteed if the power to the target system is shut down during debugging. Note that the POC function cannot be emulated.

➢ After change (underlined portion)

(4) Resetting the target device by power-on clear (POC) only

Figure 4-18 illustrates the circuit connection for the case where the target device is only reset via POC without using the reset pin. RESET_OUT is valid only when the debugger is running or during flash programming.

Even if power supply to the target system is turned off during debugging, pseudo POC function emulation is available because RESET_OUT becomes active. Note that there is an error of ±1 V between the POC detection voltage and the target system voltage.

➢ Location 2

(13) in **4.2.7 Cautions on debugging** (p. 89)

➢ Before change

(13) Emulation of POC function

The POC function of the target device cannot be emulated. Make sure that the power to the target system is not shut down during debugging

➢ After change

(13) Emulation of POC function

If power supply to the target system is turned off during debugging, the target device enters the reset state by the RESET_OUT pin of MINICUBE2. Consequently, the target device's POC function performs pseudo emulation. Note that there is an error of ±1 V between the POC detection voltage and the target system voltage.

5.9 Addition of cautions related to debugging (78K0)

➢ Location

4.2.7 Cautions on debugging (p. 89)

➢ Added description

(14) Device with/without on-chip debug function

Only the devices with the on-chip debug function can be debugged. See the user's manual of the target device for checking whether it is equipped with the on-chip debug function.

To debug a device without the on-chip debug function, perform debugging by using an upper-compatible product. The following shows an example when using the 78K0/KF2.

Target Device	On-Chip Debug Function	Device for Debugging	Device File (DF) Used for Debugging
μPD78F0544	Not equipped	μPD78F0547D (Set the IMS and IXS registers to values according to the target device.)	DF for μPD78F0544
μPD78F0545			DF for μPD78F0545
μPD78F0546			DF for μPD78F0546
μPD78F0547			DF for μPD78F0547

6. Revision History

Document Number	Issued on	Description
ZUD-CD-06-0046	March 20, 2006	1st edition
ZUD-CD-06-0046-1	March 31, 2006	- Upgrade of PRM78F0893 from V1.01 to V1.02 in the table in **4.1 78K0 microcontrollers** - Upgrade of firmware from V1.00 to V2.00 in the table in **4.2 V850 microcontrollers**
ZUD-CD-06-0046-2	April 24, 2006	- Addition of descriptions of 78K0S microcontrollers - Correction of ID78K0-QB version from V1.00 to V2.93 in the table in **4.3 78K0S microcontrollers**
ZUD-CD-06-0046-3	July 14, 2006	- Addition of descriptions of 78K0R microcontrollers - Addition of 78K0S restrictions No. 8 to No. 10 - Update of tables in **4.1 78K0 microcontrollers**, **4.2 V850 microcontrollers** and **4.3 78K0S microcontrollers**
ZUD-CD-06-0046-4	August 24, 2006	- Addition of corrections of restriction No. 9 - Update of tables in **4.1 78K0 microcontrollers**, **4.2 V850 microcontrollers** and **4.3 78K0S microcontrollers**
ZUD-CD-07-0007	January 16, 2007	- Addition of corrections to restrictions No. 11 to No.13 - Addition of restrictions and changed/added specifications No. 14 to No. 18 - Update of tables in **4.1 78K0 microcontrollers**, **4.2 V850 microcontrollers** and **4.3 78K0S microcontrollers** - Addition of **5. Changes to User's Manual**