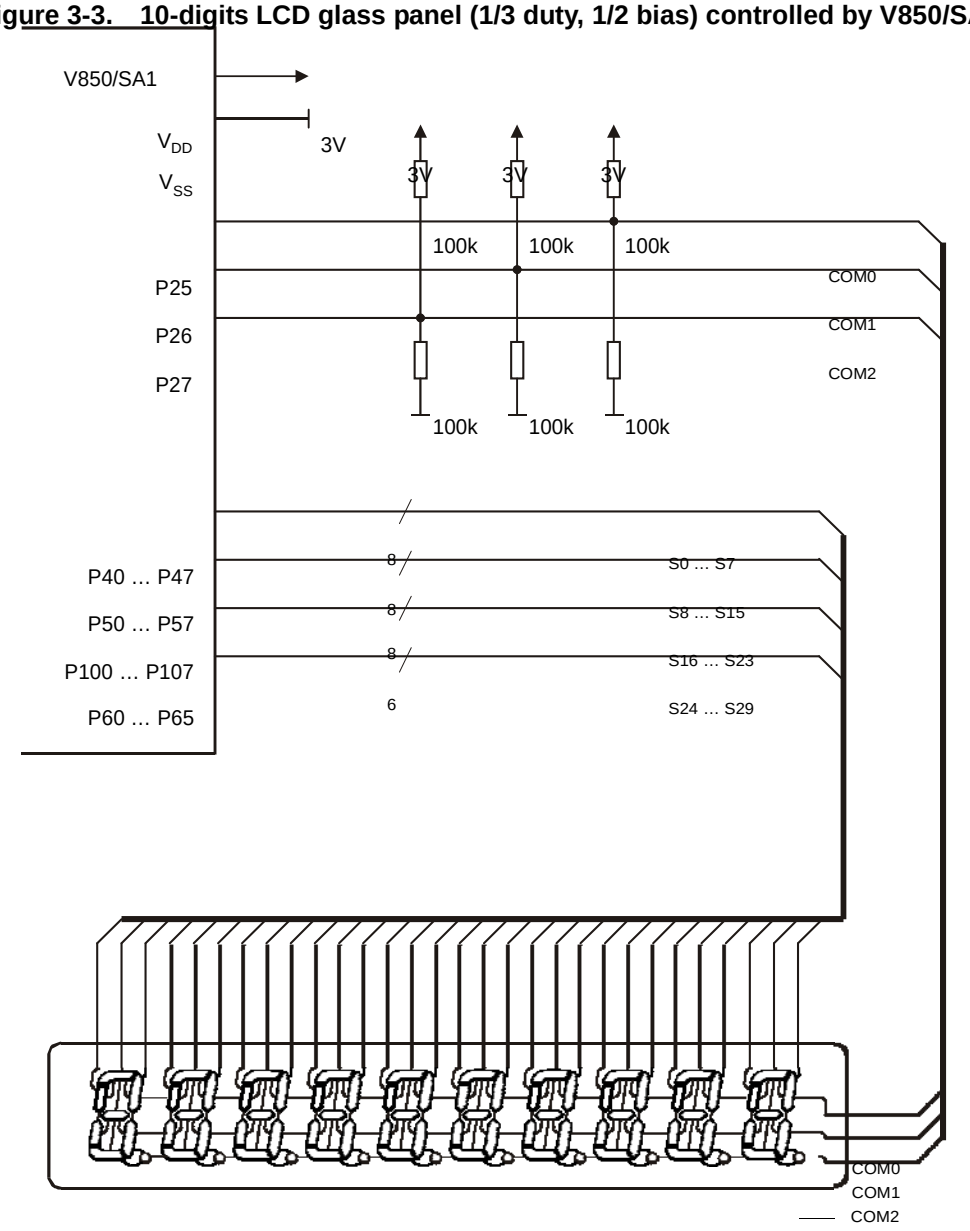
NEC芯片原理图_V850/SAI CPU 驱动LED数码管8*8图例

For 1/2 bias control only the common lines have to drive a 1/2 bias voltage (see Figure 2-3). In the
example the three common lines are realized by port pins P25 to P27, which are provided with input hysteresis capability.

The segment lines, in case of 1/2 bias mode, have to drive just a low- or high-level output voltage. This can be done with any port, whose mode can be set to output. In the example the port pins P40 to P47, P50 to P57, P100 to P107, and P60 to P65 are selected for segments control. All these ports do not provide an input hysteresis, but can be set to output mode.

The examples diagram is shown in Figure 3-3.

Figure 3-3. 10-digits LCD glass panel (1/3 duty, 1/2 bias) controlled by V850/SA1



LCD glass panel, V_{LCD} = 3V, ½ bias

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